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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

William P. MOORE, et al.

Serial No.: 09/805,200 Group Art Unit: 2183

Filed: March 14, 2001 Examiner: Shane F. GERSTL

For: MICROPROCESSOR INCLUDING MICROCODE UNIT THAT ONLY CHANGES THE VALUE OF CONTROL SIGNALS REQUIRED FOR THE CURRENT CYCLE OPERATION FOR REDUCED POWER CONSUMPTION AND METHOD THEREOF

Honorable Commissioner of Patents
Alexandria, VA 22313-1450

APPELLANT'S BRIEF ON APPEAL

Sir:

Appellants respectfully appeal the final rejection of claims 1-4, 6, 9, 20, and 23-30 in the Office Action dated December 13, 2004. A Notice of Appeal was filed timely on Monday, February 14, 2005, since the due date of February 13, 2005 fell on a weekend.

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corporation, assignee of 100% interest of the above-referenced patent application.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-4, 6, 9, 20, and 23-30, all of the claims in the Application, are set forth fully in the attached Appendix.

Claims 1-4, 6, 9, 20, and 23-30 stand rejected on prior art grounds.

Particularly, Claim 20 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Damouny (U.S. Patent No. 4,713,750). Claims 1-4, 6, 9, and 23-30 stand rejected under 35 U.S.C. § 103(s) as being unpatentable over Damouny in view of Thoma (U.S. Patent No. 4,484,268).

Appellants respectfully appeal the rejections of Claim 20 under 35 U.S.C. § 102(b) as being anticipated by Damouny and Claims 1-4, 6, 9, and 23-30 under 35 U.S.C. § 103(s) as being unpatentable over Damouny in view of Thoma, which are the sole issues in this Appeal.

IV. STATUS OF AMENDMENTS

An Amendment under 37 C.F.R. § 1.116 was filed on December 13, 2004. Claim 23 was amended merely to add proper punctuation (i.e., a "colon") after the term "*comprising*" in line 2 of claim 23.

An Advisory Action mailed January 4, 2005 entered the Amendment under 37 C.F.R. § 1.116 filed on December 13, 2004, but held claims 1-4, 6, 9, 20, and 23-30 unpatentable.

A Notice of Appeal was filed timely on Monday, February 14, 2005, since the due date of February 13, 2005 fell on a weekend.

Therefore, the claims are pending as set forth in the Appendix.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The invention, as set forth and defined by independent claim 1 is directed to a microprocessor, a microcode unit in a microprocessor, and a method of providing a state machine decoding.

Referring to the exemplary embodiments of the invention depicted in Figures 3A-5, a microprocessor according to an illustrative aspect of the present invention, as exemplarily defined by independent claim 1, includes a microprocessor, including a microcode unit (e.g., 32; see specification at page 7, lines 27-29; and page 8, lines 1-4) for outputting control signals, for each of a plurality of instructions, required by the microprocessor for executing the instructions. Referring to Figure 3B, the microcode unit (e.g., sub-unit 321 of microcode unit 32) includes an instruction address input (schematically shown in Figures 3B) for receiving an instruction address (e.g., address comparator 3211 for receiving a microcode address signal; see specification at page 8, lines 20-22), a control variable input (schematically shown in Figures 3B) for receiving a control variable (e.g., logic signals; see specification at page 9, lines 6-10) corresponding to a current state of the microprocessor, a control signal input (schematically shown in Figures 3B) for receiving all the control signals output by the microcode unit for an immediately preceding instruction (e.g., previous control signals; see specification at page 9, lines 2-5) and a plurality of embedded logic circuits (e.g., 3215) each dedicated for evaluating one unique type of instruction received by the microcode unit and for setting the control signals required for executing the received instruction (e.g., see specification at page 9, lines 6-10).

Referring now to Figure 3C, as exemplarily defined by claim 2, each of the embedded logic circuits (e.g., 3215) can include a table (e.g., 32151, as shown in Figures 3C) for performing a table lookup in response to a received instruction, and a controller (schematically

shown in Figures 3C) responsive to the control variable, the control signals for an immediately preceding instruction, and to the table lookup for controllably setting each of the control signals required by the microprocessor for executing the received instruction (e.g., see specification at page 12, lines 8-17).

Referring again to Figure 3B, as exemplarily defined by claim 3, the controller can include means for setting a control signal to a "1" (e.g., 3212) regardless of its immediately preceding value, means for setting a control signal to a "0" (e.g., 3213) regardless of its immediately preceding value, and means for not modifying a control signal from its immediately preceding value (e.g., 3214)(see also, specification at page 12, lines 18-23; see also page 8, lines 20-30 and page 9, line 1).

Referring again to Figure 3B, as exemplarily defined by claim 4, the controller can further include means for setting a control signal to a data state (e.g., see specification at page 12, lines 22-23).

Referring again to Figure 3B, as exemplarily defined by claim 6, the controller also can include means for determining which of the control signals are not to be modified for each instruction (e.g., see specification at page 12, lines 11-27).

Referring again to Figure 3C, as exemplarily defined by claim 9, a microcode unit (e.g., 32; see specification at page 7, lines 27-29; and page 8, lines 1-4) in a microprocessor, for outputting control signals (e.g., see Figure 3A), for each of a plurality of instructions, required by the microprocessor for executing the instructions. The microcode unit (e.g., sub-unit 321 of microcode unit 32) can include an instruction address input (e.g., address comparator 3211 for receiving a microcode address signal; see specification at page 8, lines 20-22) for receiving an instruction address, a control variable input (schematically shown in Figures 3B) for receiving a

control variable (e.g., logic signals; see specification at page 9, lines 6-10) corresponding to a current state of the microprocessor, a control signal input (schematically shown in Figures 3B) for receiving all the control signals output by the microcode unit for an immediately preceding instruction (e.g., previous control signals; see specification at page 9, lines 2-5), and a plurality of embedded logic circuits (e.g., 3215) each dedicated for evaluating one unique type of instruction received by the microcode unit and for setting the control signals required for executing the received instruction (e.g., see specification at page 9, lines 6-10).

Referring to Figures 3D-4B, as exemplarily defined by independent claim 20, a method of providing a state machine decoding, includes decoding a current opcode (e.g., step 301) to provide a decode (e.g., see specification at page 13, line 30, and page 14, lines 1-8), setting required functions signals (e.g., step 302; see specification at page 14, lines 8-9), setting exclusive functions outside of the current opcode to a previous state (e.g., step 303; see specification at page 14, lines 10-11), and latching results of the decode (e.g., step 304; see specification at page 14, line 11).

Turning again to the microprocessor according to the claimed invention, as exemplarily defined by claim 23, and referring again to Figure 3C, each of the plurality of embedded logic circuits includes a controller (schematically shown in Figures 3C) for controllably setting each of the control signals required by the microprocessor for executing the received instruction (e.g., see specification at page 12, lines 11-23).

Referring again to Figure 3C, as exemplarily defined by claim 24, each of the plurality of embedded logic circuits includes a controller (schematically shown in Figures 3C) for controllably setting only each of the control signals required by the microprocessor for executing the received instruction (e.g., see specification at page 12, lines 11-23).

Referring again to Figure 3C, as exemplarily defined by claim 25, each of the plurality of embedded logic circuits includes a table (e.g., 32151, as shown in Figures 3C) that performs a table lookup in response to a received instruction (e.g., see specification at page 12, lines 8-17).

Referring again to Figure 3C, as exemplarily defined by claim 26, the controller is responsive to the control variable, the control signals for an immediately preceding instruction, and to the table lookup (e.g., see specification at page 12, lines 18-23; see also page 8, lines 20-30 and page 9, line 1).

Referring again to Figures 3B and 3C, as exemplarily defined by claim 27, the controller includes means for maintaining a control signal at an immediately preceding value of the control signal (see also, specification at page 12, lines 18-23; see also page 8, lines 20-30 and page 9, line 1).

Referring again to Figures 3B and 3C, as exemplarily defined by claim 28, the controller further includes means (e.g., 3212) for setting a control signal to a "1" regardless of an immediately preceding value of the control signal, and means (e.g., 3213) for setting a control signal to a "0" regardless of an immediately preceding value of the control signal (see also, specification at page 12, lines 18-23; see also page 8, lines 20-30 and page 9, line 1).

Referring to Figures 3B and 3C, as exemplarily defined by claim 29, the controller further includes means (e.g., 3214) for setting a control signal to a data state (e.g., see specification at page 12, lines 22-23).

Referring to Figures 3B and 3C, as exemplarily defined by claim 30, the controller can further include means (e.g., 3214) for determining at least one of the control signals to be maintained for each instruction (see also, specification at page 12, lines 18-23; see also page 8, lines 20-30 and page 9, line 1).

In the claimed invention, in addition to the "0" or "1" value which can be set for each control signal, the previous value can also be set, thereby reducing the power within the microprocessor (e.g., see specification at page 10, lines 2-5).

Specifically, since each function is a function of a microcode address, by only changing the value of control signals that are absolutely required for that particular microcode address (e.g., ADD, STORE, MULT etc. as determined by the decoding), the power of the microprocessor can be minimized since node toggle, as discussed above, is greatly reduced as compared to the conventional machines and systems (e.g., see specification at page 10, lines 6-11).

For example, in an exemplary embodiment of the claimed invention, the power savings was on the order of about 30-40% over the conventional systems. Hence, if the function remains the same from a previous opcode to the next opcode (and hence from cycle-to-cycle), then the previous value may be maintained again, and no node toggle results since values are not being changed from high to low or from low to high (e.g., see specification at page 10, lines 11-16).

Thus, with the claimed invention, each opcode becomes a function of the previous opcode and only conflicting (e.g., required) control signals must be resolved, thereby greatly reducing power consumption (e.g., see specification at page 10, lines 17-19).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues presented for review by the Board of Patent Appeals and Interferences are whether Claim 20 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Damouny and whether Claims 1-4, 6, 9, and 23-30 stand rejected under 35 U.S.C. § 103(s) as being unpatentable over Damouny in view of Thoma.

VII. ARGUMENT

A. THE EXAMINER'S POSITION

In the Response to Arguments of the final Office Action mailed October 13, 2004, the Examiner stated that "*the features upon which Applicant relies (i.e., that only the required control signals are resolved or changed) are not recited in the rejected claim(s)...since the claims read that the required control signals are changed, the reference must teach that these control signals are changed, but may also disclose other control signals that are changed since the claim mentions nothing about the other control signals*" (see Office Action mailed October 13, 2004, at page 13, numbered paragraph 24; emphasis added).

In the Response to Arguments, the Examiner further stated that "*a recitation of intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim*" (see Office Action mailed October 13, 2004, at page 14, numbered paragraph 25; emphasis added).

In the Advisory Action mailed January 4, 2005, the Examiner indicated that the request for reconsideration had been considered but did not place the application in condition for allowance because:

> *The argument for claim 1 is not persuasive. Applicant argues that it would not be obvious to modify Damouny in view of Thoma since, by teaching that every control signal is modified for each instruction, Damouny would teach away from the claimed invention and that if a modification were made to meet the claim, it would require a change in the principle operation (sic) of the device of Damouny. The Examiner fails to see how this is the case for this specific claim.*

As stated in the previous Action, claim 1 only defines that the system has circuits for "setting the control signals required for executing said received instruction", which means that control needed for execution is set but clearly does not give language requiring that only the control signals needed for execution are set where the other signals are not set as claimed in dependent claim 24. This language along with the "comprising" transitory phrase facilitates the interpretation that the control signals required are set as well as any other control signals, which may actually be set to retain the previous value and thus functionality are not set yet physically are set. Perhaps applicant believes that the fact Damouny modifies every control signal for each instruction teaches away from the claimed invention because of the limitation that previous control signals are received. The Examiner asserts that it is perfectly reasonable for the control signals to be set for each instruction and still be based on previous control signals such as signal 182 of figure 1A.

(See Advisory Action mailed January 4, 2005 at continuation Sheet (PTOL-303).

B. APPELLANT'S POSITION

To summarize, Appellants submit that the Examiner's position is flawed as a matter of fact and law. Thus, Claim 20 is not anticipated by, or rendered obvious from, Damouny, and Claims 1-4, 6, 9, and 23-30 also are not rendered obvious from Damouny in view of Thoma.

i) Claim 20 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Damouny.

For the following reasons, Appellants respectfully submit that the Examiner's position is flawed as a matter of fact and law, and therefore, traverse this rejection.

For example, claim 20 recites, *inter alia*, a method of providing a state machine decoding, comprising:

decoding a current opcode to provide a decode;
setting required functions signals;
setting exclusive functions outside of the current opcode to a previous state; and
latching results of the decode (emphasis added).

The Office Action alleges that Damouny discloses a method of providing a state machine decoding including setting required functions signals, as claimed. Particularly, the Examiner alleges that Damouny discloses that the pointers are necessary for execution and thus are required functions signals (see Office Action mailed October 13, 2004, at page 2, numbered paragraph 6(b); emphasis added).

However, Appellants respectfully submit that the Examiner is mischaracterizing the Damouny reference.

That is, disclosing generally that the pointers are necessary for execution does not mean that Damouny discloses or suggests setting only the required function signals, as claimed.

On the contrary, Damouny does not disclose, suggest, or even contemplate *which* of the function signals would be set. Indeed, Damouny does not disclose, suggest, or even address the problems being solved by the claimed invention.

In comparison, the claimed invention discloses that, since each function is a function of a microcode address, by only changing the value of control signals that are absolutely *required* for that particular microcode address (e.g., ADD, STORE, MULT etc. as determined by the decoding), the power of the microprocessor can be minimized and node toggle can be greatly reduced as compared to the conventional machines and systems (e.g., see specification at page 10, lines 6-11).

For at least the foregoing reasons, Appellants respectfully submit that Damouny neither discloses nor suggests all of the features of independent claim 20, and therefore, respectfully

request that the Examiner withdraw this rejection and permit claim 20 to pass to immediate allowance.

ii) Claims 1-4, 6, 9, and 23-30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Damouny in view of Thoma.

For the following reasons, Appellants respectfully submit that the Examiner's position is flawed as a matter of fact and law, and therefore, traverse this rejection.

As set forth above, in the Response to Arguments, the Examiner alleges that "*the features upon which Applicant relies (i.e., that only the required control signals are resolved or changed) are not recited in the rejected claim(s)...since the claims read that the required control signals are changed, the reference must teach that these control signals are changed, but may also disclose other control signals that are changed since the claim mentions nothing about the other control signals*" (see Office Action at page 13, numbered paragraph 24; emphasis added).

However, Appellants respectfully note that claim 24 clearly recites that "*each of the plurality of embedded logic circuits comprises a controller for controllably setting **only** each of the control signals **required** by the microprocessor **for executing said received instruction***" (emphasis added). A detailed discussion of the rejection of claim 24 is set forth below.

Also as set forth above, in the Response to Arguments, the Examiner alleges that "*a recitation of intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim*" (see Office Action at page 14, numbered paragraph 25; emphasis added).

However, for the reasons set forth below, Appellants respectfully submit that, even (*arguendo*) if arguments of intended use have been asserted, the applied references are **not** capable of performing the intended use of the claimed invention, and indeed, do not disclose, suggest, or even mention the intended use and/or advantages of the claimed invention.

For the reasons set forth below, Appellants respectfully reiterate that Damouny and Thoma, either alone or in combination, do not disclose, suggest, or even mention these features of the claimed invention, or for that matter, the advantages derived from the unique combination of structural features recited in the claimed invention.

For example, as mentioned above, the claimed invention provides a novel and unique combination of elements in which, since each function is a function of a microcode address, by **only** changing the value of control signals that are absolutely required for that particular microcode address (i.e., as exemplarily defined by dependent claim 24) (e.g., ADD, STORE, MULT etc. as determined by the decoding), the power of the microprocessor can be minimized since node toggle, as discussed above, is greatly reduced as compared to the conventional machines and systems (e.g., see specification at page 10, lines 6-11). That is, in an exemplary aspect of the claimed invention, each opcode becomes a function of the previous opcode and only conflicting (e.g., required) control signals must be resolved, thereby greatly reducing power consumption (e.g., see specification at page 10, lines 17-19).

With respect to independent claim 1, Appellants reiterate that independent claim 1 would not have been obvious from Damouny in view of Thoma.

a) Independent Claim 1

For example, independent claim 1 recites, *inter alia*, a microprocessor, comprising:

> a microcode unit for outputting control signals, for each of a plurality of instructions, required by said microprocessor for executing said instructions, the microcode unit comprising:
>
> > *an instruction address input for receiving an instruction address;*
> > ***a control variable input** for receiving a control variable corresponding to **a current state** of the microprocessor;*
> > ***a control signal input** for receiving **all the control signals output** by the microcode unit **for an immediately preceding instruction**; and*
> > *a plurality of embedded logic circuits each dedicated for evaluating one unique type of instruction received by the microcode unit and for setting the control signals **required** for executing said received instruction* (emphasis added).

Appellants submits that it would not have been obvious to modify Damouny in view of Thoma since, by teaching that every control signal is modified for each instruction, Damouny would teach away from the claimed invention. Moreover, if Damouny were modified to arrive at the claimed invention, such a modification clearly would require a change in the principle of operation of the device of Damouny.

As mentioned above, in the Advisory Action mailed January 4, 2005, the Examiner stated that:

> *The argument for claim 1 is not persuasive. Applicant argues that it would not be obvious to modify Damouny in view of Thoma since, by teaching that every control signal is modified for each instruction, Damouny would teach away from the claimed invention and that if a modification were made to meet the claim, it would require a change in the principle operation (sic) of the device of Damouny. The Examiner fails to see how this is the case for this specific claim. As stated in the previous Action, claim 1 only defines that the system has circuits for "setting the control signals required for executing said received instruction", which means that control needed for execution is set but clearly does not give*

> *language requiring that only the control signals needed for execution are set where the other signals are not set as claimed in dependent claim 24. This language along with the "comprising" transitory phrase facilitates the interpretation that the control signals required are set as well as any other control signals, which may actually be set to retain the previous value and thus functionality are not set yet physically are set. Perhaps applicant believes that the fact Damouny modifies every control signal for each instruction teaches away from the claimed invention because of the limitation that previous control signals are received. The Examiner asserts that it is perfectly reasonable for the control signals to be set for each instruction and still be based on previous control signals such as signal 182 of figure 1A.*

(See Advisory Action mailed January 4, 2005 at continuation Sheet (PTOL-303); emphasis added).

As mentioned above, independent claim 1 recites, *inter alia*, a microcode unit including "*a control signal input for receiving **all** the control signals output by the microcode unit for an immediately preceding instruction*" (emphasis added).

However, with respect to the signal 182 of Damouny, Appellants respectfully submit that Damouny merely discloses that "*[t]he input signals that control the internal state of the branch PLA arrive on the bus 182 as the branch select field and on the bus 184 representing various internal and external branch conditions such as overflow, interrupt, abort, etc.*" (see Damouny at column 4, lines 57-61; see also Figure 1A), not that a control signal input receives "***all** the control signals output by the microcode unit for an immediately preceding instruction*" as claimed in claim 1.

Thus, Appellants respectfully submit that Damouny and Thoma, either alone or in combination, do not disclose or suggest all of the features of independent claim 1 of the present application.

b) Dependent Claims 2-4 and 6

Appellants also reiterate that dependent claims 2-4 and 6 also should be patentable at least by virtue of their dependency from claim 1, as well as for the additional recitations recited therein.

Dependent Claim 3

For example, with respect to dependent claim 3, in the Response to Arguments, the Examiner alleges that "*[t]he third limitation has been given patentable weight counter to what the Applicant thought was the examiner's intention and the examiner had wished only to point out that regarding the first two limitations, the phrase "regardless of the preceding value" is inherently met since the signals will be either set based on the previous value or not based on the value. Regarding the third limitation, when the control signal of mention does not change from one instance to the next, the control signal is set to the same value as before and is not modified from the previous value, but is modified to retain the value*" (see Office Action mailed October 13, 204, at page 14, numbered paragraph 26; emphasis original).

Dependent claim 3 recites, *inter alia*, that the controller includes:

> *means for setting a control signal to a "1" regardless of its immediately preceding value;*
> *means for setting a control signal to a "0" regardless of its immediately preceding value; and*
> *means for not modifying a control signal from its immediately preceding value* (emphasis added).

The specification clearly describes that, in addition to the "0" or "1" value which can be set for each control signal, the previous value can also be set, thereby reducing the power within the microprocessor (e.g., see specification at page 10, lines 2-5).

As mentioned above, the Examiner alleges that "*when the control signal of mention does not change from one instance to the next, the control signal is set to the same value as before and is not modified from the previous value, but is modified to retain the value*".

However, Damouny and Thoma, alone or in combination, do not disclose or suggest maintaining and/or retaining the previous value. Instead, these references simply teach that every control signal is modified for each instruction.

Such clearly does not imply that Damouny or Thoma disclose "*means for **not** modifying a control signal from its immediately preceding value*" as claimed. Indeed, the Examiner has not cited any structure, equivalents thereof, or identity of function necessary for the claimed "*means for not modifying a control signal from its immediately preceding value*".

In comparison, the disclosure of the present application exemplarily describes that the output signal of the address comparator 3211 is issued to AND gate 3212 (e.g., for the "1" block), AND gate 3213 (e.g., for the "0" block), and to AND gate 3214 (e.g., see specification at page 8, lines 24-30 and page 9, line 1).

Thus, Appellants respectfully submit that claim 3 is patentable over Damouny and Thoma, either alone or in combination.

Dependent Claim 6

With respect to claim 6, in the Response to Arguments, the Examiner alleges that "*Applicant has argued that since Damouny discloses that every control signal is modified for each instruction, no determination would need to be made on which control signals are to be modified and which are not to be modified. As Applicant has admitted, Damouny discloses automatically modifying every control signal for each instruction. This would then inherently mean that there is **means for determining** that **no** control signals are to **not** be modified since*

*the system automatically modifies **all** control signals, whether the determination is hardwired and is the same determination every time or otherwise*" (see Office Action at page 15, numbered paragraph 27; emphasis added).

Appellants respectfully disagree with the Examiner's position, for several reasons.

Dependent claim 6 recites, *inter alia*, "*means for determining which of the control signals are not to be modified for each instruction*" (emphasis added).

To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency may not be established by probabilities and statistics. The mere fact that a certain thing may result from a given set of circumstances is not sufficient (see M.P.E.P. § 2112; see also *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999); emphasis added).

As mentioned above, Damouny discloses automatically modifying every control signal for each instruction. It would not be inherent in Damouny to provide a structural element which determines that "*no control signals are to not be modified*", as alleged by the Examiner, simply because the system automatically modifies all control signals.

On the contrary, since all control signals in Damouny are automatically modified, there is no need (i.e., it is not necessary) to even make such a determination. As mentioned above, inherency requires that the missing element **necessarily** flows from the teachings of the applied art.

Damouny clearly does not necessarily disclose or suggest making such a determination, or for that matter, any structural features which would make such a determination. Indeed, the

Examiner has not cited any structure, equivalents thereof, or identity of function necessary for the claimed "means for determining".

Moreover, Damouny does not, and cannot, modify some (i.e., not all) of the control signals. Thus, it clearly is unreasonable to interpret Damouny as inherently including a feature which it does not need to perform (or cannot perform).

Appellants also submit that it clearly is unreasonable to interpret Damouny as inherently including the claimed feature even though it has no use for such a feature. In fact, if Damouny were modified to include such features, such modifications would change the principle of operation of the Damouny reference.

For the foregoing reasons, Appellants respectfully submit that Damouny and Thoma, either alone or in combination, do not disclose or suggest all of the features of claim 6.

c) Dependent Claims 23-30

With respect to claims 23-30, the Examiner rejects these claims as being unpatentable over Damouny in view of Thoma. However, Appellants respectfully submit that claims 23-30 would not have been obvious from Damouny and Thoma, alone or in combination. Therefore, Appellants traverse the rejection of these claims.

Dependent Claim 24

For example, dependent claim 24 recites, *inter alia*, that "*each of the plurality of embedded logic circuits comprises a controller for controllably setting **only** each of the control signals required by the microprocessor for executing said received instruction*" (emphasis added).

The Examiner alleges that Figure 1A of Damouny discloses this feature of the claimed invention. However, as the Examiner also acknowledged in the Office Action mailed on April

16, 2004, in the final Office Action mailed October 13, 2004, and in the Advisory Action mailed January 4, 2005, Damouny discloses that "*every control signal is modified for each instruction*".

Thus, Damouny clearly does not disclose or suggest "*a controller for controllably setting **only** each of the control signals required by the microprocessor for executing said received instruction*" as recited in claim 24.

Indeed, the Examiner acknowledged this distinction between the modifying every control signal for each instruction and "*controllably setting **only** each of the control signals required by the microprocessor for executing said received instruction*", as recited in claim 24 (see Advisory Action at Continuation Sheet).

Dependent Claim 27

As another example, dependent claim 27 recites, *inter alia*, that "*the controller includes means for maintaining a control signal at an immediately preceding value of said control signal*" (emphasis added).

However, as mentioned above, Damouny and Thoma, alone or in combination, do not disclose or suggest maintaining and/or retaining the previous value.

Instead, the references simply teach that every control signal is modified for each instruction. Such clearly does not imply that Damouny or Thoma disclose "*means for maintaining a control signal at an immediately preceding value of said control signal*" as claimed.

Indeed, the Examiner has not cited any structure, equivalents thereof, or identity of function necessary for the claimed "*means for maintaining a control signal at an immediately preceding value of said control signal*".

Thus, Appellants respectfully submit that claim 27 is patentable over Damouny and Thoma, either alone or in combination.

Dependent Claim 30

On the other hand, dependent claim 30 recites, *inter alia*, "means for determining at least one of said control signals to be maintained for each instruction" (emphasis added).

However, as mentioned above, Damouny and Thoma, alone or in combination, do not disclose or suggest maintaining and/or retaining the previous value.

Instead, the references simply teach that **every** control signal is modified for each instruction. Such clearly does not imply that Damouny or Thoma disclose "*means for determining*" as claimed.

Indeed, the Examiner has not cited any structure, equivalents thereof, or identity of function necessary for the claimed "*means for determining*".

Thus, Appellants respectfully submit that claim 30 is patentable over Damouny and Thoma, either alone or in combination.

For the foregoing reasons, Appellants respectfully submit that Damouny and Thoma, either alone or in combination, do not disclose or suggest all of the features of the claimed invention.

Therefore, the Examiner respectfully is requested to reconsider and withdraw the rejection of these claims and permit claims 1-4, 6, 9, 20, and 23-30 to pass to immediate allowance.

VIII. CONCLUSION

In view of the foregoing, Appellant submits that claims 1-4, 6, 9, 20, and 23-30, all the claims presently pending in the application, are patentably distinct from the prior art of record and in condition for allowance. Thus, the Board is respectfully requested to remove the rejections of claims 1-4, 6, 9, 20, and 23-30.

Please charge any deficiencies and/or credit any overpayments necessary to enter this paper to Assignee's Deposit Account No. 09-0456.

Respectfully Submitted,

Date: **April 14, 2005**

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CLAIMS APPENDIX

1. (Previously presented) A microprocessor, comprising:

a microcode unit for outputting control signals, for each of a plurality of instructions, required by said microprocessor for executing said instructions, the microcode unit comprising:

an instruction address input for receiving an instruction address;

a control variable input for receiving a control variable corresponding to a current state of the microprocessor;

a control signal input for receiving all the control signals output by the microcode unit for an immediately preceding instruction; and

a plurality of embedded logic circuits each dedicated for evaluating one unique type of instruction received by the microcode unit and for setting the control signals required for executing said received instruction.

2. (Original) The microprocessor according to claim 1, wherein each of the embedded logic circuits includes:

a table for performing a table lookup in response to a received instruction; and

a controller responsive to the control variable, the control signals for an immediately preceding instruction, and to the table lookup for controllably setting each of the control signals required by the microprocessor for executing said received instruction.

3. (Original) The microprocessor of claim 2, wherein the controller includes:

means for setting a control signal to a "1" regardless of its immediately preceding value;

means for setting a control signal to a "0" regardless of its immediately preceding value; and

means for not modifying a control signal from its immediately preceding value.

4. (Original) The microprocessor of claim 3, wherein the controller further includes:

means for setting a control signal to a data state.

5. (Canceled).

6. (Previously presented) The microprocessor according to claim 1, further comprising means for determining which of the control signals are not to be modified for each instruction.

7-8. (Canceled).

9. (Previously presented) A microcode unit in a microprocessor, for outputting control signals, for each of a plurality of instructions, required by said microprocessor for executing said instructions, the microcode unit comprising:

an instruction address input for receiving an instruction address;

a control variable input for receiving a control variable corresponding to a current state of the microprocessor;

a control signal input for receiving all the control signals output by the microcode unit for an immediately preceding instruction; and

a plurality of embedded logic circuits each dedicated for evaluating one unique type of instruction received by the microcode unit and for setting the control signals required for executing said received instruction.

10-19. (Canceled).

20. (Original) A method of providing a state machine decoding, comprising:

decoding a current opcode to provide a decode;

setting required functions signals;

setting exclusive functions outside of the current opcode to a previous state; and

latching results of the decode.

21-22. (Canceled).

23. (Previously presented) The microprocessor of claim 1, wherein each of the plurality of embedded logic circuits comprises:

a controller for controllably setting each of the control signals required by the microprocessor for executing said received instruction.

24. (Previously presented) The microprocessor of claim 1, wherein each of the plurality of embedded logic circuits comprises a controller for controllably setting only each of the control signals required by the microprocessor for executing said received instruction.

25. (Previously presented) The microprocessor of claim 1, wherein each of the plurality of embedded logic circuits comprises a table that performs a table lookup in response to a received instruction.

26. (Previously presented) The microprocessor of claim 25, wherein said controller is responsive to the control variable, the control signals for an immediately preceding instruction, and to the table lookup.

27. (Previously presented) The microprocessor of claim 23, wherein the controller includes means for maintaining a control signal at an immediately preceding value of said control signal.

28. (Previously presented) The microprocessor of claim 27, wherein the controller further includes:

means for setting a control signal to a "1" regardless of an immediately preceding value of said control signal; and

means for setting a control signal to a "0" regardless of an immediately preceding value of said control signal.

29. (Previously presented) The microprocessor of claim 28, wherein the controller further comprises means for setting a control signal to a data state.

30. (Previously presented) The microprocessor according to claim 1, further comprising means for determining at least one of said control signals to be maintained for each instruction.

EVIDENCE APPENDIX

Not applicable.

RELATED PROCEEDINGS APPENDIX

Not applicable.